Eureka Technology

ispLeverCORE Approved

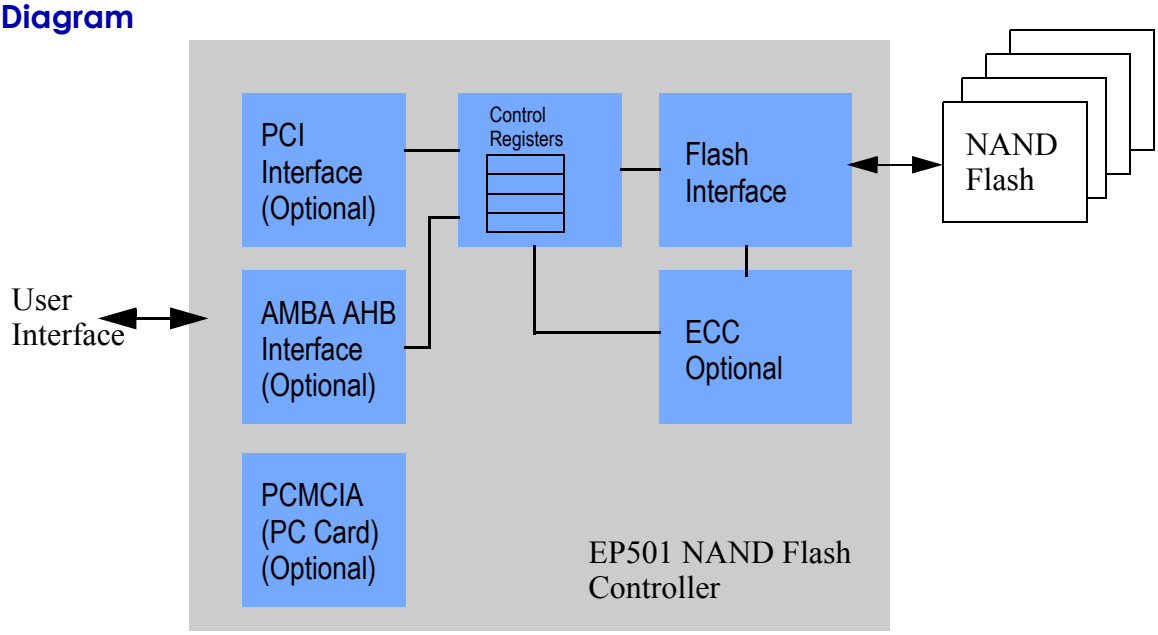
Product Summary

EP501 NAND Flash Controller

FEATURES

- Supports up to 4 banks of NAND Flash devices.
- Each bank contains up to 5 NAND Flash connected in parallel for a total of 20 NAND Flash devices.
- Simple user interface designed for easy on-chip integration.
- Options to provide PCI, AMBA AHB, PCMCIA, Cardbus or CompactFlash bus interface.
- Large Flash memory space can be accessed using data and index register method.
- Programmable access timing, NAND Flash size, data width and number of banks.
- Supports large block and small block NAND Flash devices.
- User has full access to spare data in NAND Flash device.
- Optional single-bit correction double bit detection error correction code (ECC).
- Option to apply ECC protection on per word or per page basis.
- Error logging with ECC correction and detection.
- Interrupt generation based on ECC error.
- Designed for ASIC and FPGA implementations.
- Fully static design with edge-triggered flip-flops.

Block Diagram



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DESCRIPTIONS

The EP501 NAND Flash controller provides an easy interface for user to access NAND Flash devices. Typical NAND Flash devices are accessed through complicated sequence of command, address, data, and confirmation protocols. The EP501 manages all the hardware protocols and allows the user to access NAND Flash memory simply by reading and writing control registers inside the EP501.

A very large size of NAND Flash memory can be accessed through a small number of control registers. The NAND Flash controller occupies only a small size in the system's memory space without scarifying system performance. Burst access to the NAND Flash memory is supported by the controller at full memory bandwidth. Timing parameters of the controller is fully programmable so different memory speeds are supported regardless of the operating frequency of the controller.

The EP501 supports optional error correction code (ECC) that performs single-bit error correction and double-bit error detection. There are options to provide ECC protection on per word basis or per page basis. With per word ECC, 8 bits of ECC code is generated by the core for each 32-bit data. A total for 40 bit is written to the NAND Flash for each data word. Error detection and correction are automatically performed by the core with error logging through internal control registers. The core can be configure to generate interrupt on ECC error. ECC error can also be injected into the NAND Flash device if desired for diagnostic purpose. With per page ECC, 3 bytes of ECC code is generated for every page (512 bytes) of data.

The EP501 is programmable to support both large block and small block NAND Flash devices. Memory size, bus width, access timing, and number of banks are all programmable.

Several options of user interface are available for the user to choose from. The standard version features a simple user interface that is designed for on-chip system integration. It has separate address and data buses and command signals that supports burst transfer and wait state insertion. Other standard interface buses including PCI, AMBA AHB, PCMCIA, and CardBus are available. The controller acts as a target or slave device on these buses. With these standard bus interfaces, the EP501 can be integrate seamlessly with systems built on these standards.

OPTIONAL FEATURES

The EP501 NAND Flash controller supports the following optional features per customer specification

Optional features

Error Correction Code (ECC)
Power-on boot ROM support.

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Optional features

Different user interfaces: PCI, AMBA AHB, PCMCIA, PC Card, or CompactFlash
Data width from 8 to 32 bits
More than 4 banks for memory devices.

Device Utilization

Family	Device	Utilization		Performance
		Slice	Percentage	
EC	LFEC20	1036	11%	115Mhz
XP	LFXP10	1036	21%	97Mhz
ECP2	LFE2-12E	1022	17%	115Mhz
SC	LFSC3GA15E	1043	2%	150Mhz
XP2	LFXP2-17E	1035	13%	111Mhz

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