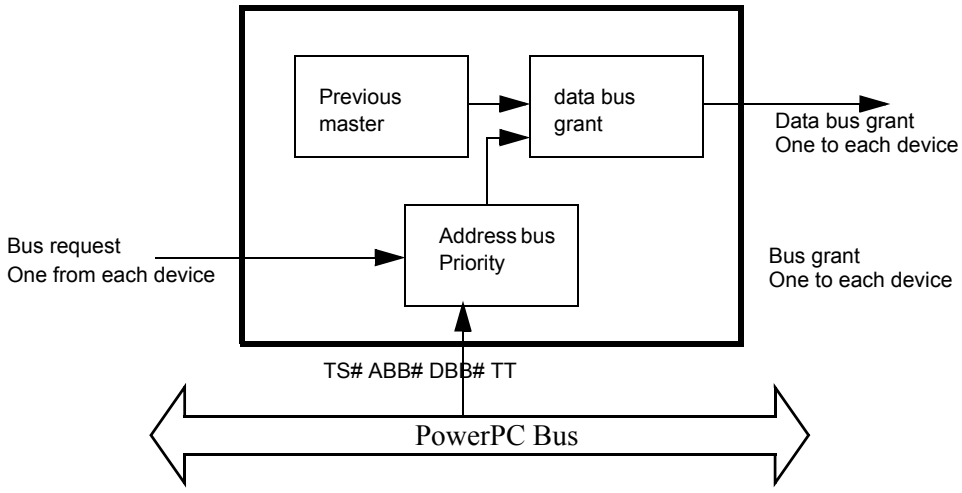
EP300 PowerPC Bus Arbiter

FEATURES

- Fully supports PowerPC™ 60x bus protocol, include PowerPC 603, 604, 740, 750 and 8260.
- Supports up to eight PowerPC bus masters with unlimited slave device support.
- Supports two outstanding bus accesses.
- Supports address only transfer and address bus retry.
- Independent address bus and data bus tenure with separate bus grant and data bus grant.
- Option for fixed priority assignment or rotating priority scheme.
- Designed for ASIC or programmable logic device implementations in various system environments.
- Fully static design with edge triggered flip-flops.
- Optimized for ispXPGA product family.

DESCRIPTIONS

The EP300 PowerPC bus arbiter provides all the necessary functions to arbitrate multiple bus masters directly connected to the PowerPC host bus. The arbiter supports separate address and data bus tenure to realize the high performance allowed by the PowerPC bus architecture. Separate address bus grant and data bus grant signals are provided for each master device on the bus. The arbiter uses sophisticated built-in state machines to coordinate the address bus tenure and the data bus tenure. At any given cycle, up to two simultaneous bus accesses are allowed.



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The EP300 PowerPC bus arbiter comes with the options of rotating priority or fixed priority schemes to meet the requirements for different system environments.

Device Utilization

Family	Device	Utilization		Performance
		Slice	Percentage	
ispXPGA	LFX1200B	17	1%	108Mhz
EC	LFEC20	54	1%	133Mhz
XP	LFXP10	54	1%	150Mhz
XP2	LFXP2-17E	54	1%	150Mhz

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